REMARKS

The present invention is an antenna and a mobile phone including an antenna. An antenna in accordance with an embodiment of the invention comprises an element as defined in paragraph [0005] of the Substitute Specification. An example of the element is illustrated in Fig. 3. The element is formed from conductor patterns 42 on a plurality of the layers including at least one buried layer of a multilayer PCB 40. The conductor patterns are in a stacked relation and may be interconnected through the PCB by vias 52.

Claims 1-4, 17-20 and 33-36 stand rejected under 35 U.S.C. §102 as being anticipated by United States Patent 6,107,970. These grounds of rejection are traversed for the following reasons.

Independent claim 1 recite:

> An antenna comprising:
> an element; and wherein
> the element is formed from conductor patterns on a plurality of layers including at least one buried layer of a multilayer PCB, and the conductor patterns are in stacked relation and interconnected through the PCB.

and

Independent claim 17 recites:

> A mobile phone including an antenna comprising an element formed from conductor patterns on a plurality of layers including at least one buried layer of a multilayer PCB, wherein the conductor patterns are in stacked relation and interconnected through the PCB.

Each of independent claims 1 and 17 substantively recite an element "formed from conductor patterns on a plurality of layers including at least one buried layer of a multilayer PCB wherein the conductor patterns are in stacked relation and

connected through the PCB." This subject matter is not disclosed by Holshouser et al for the following reasons.

The Examiner concludes regarding claims 1-4 that Holshouser et al may be construed as follows:

> Regarding Claims 1-4, and , Holshouser et al. show a mobile phone and antenna in Figures 8A and 8B and 9A and 9B, a multi-layered dielectric PCB 40 with an element 42,142 formed from conductor patterns 46a,46b and 146a,146b on a plurality of layers including at least one buried layer of the PCB, and the conductor patterns are in a stacked relation and interconnected through the PCB with conductive vias 149 extending through apertures (i.e., the PCB is apertured adjacent the element) and the element is located at the edge 48 of the PCB, all arranged as claimed.

It is submitted that the Examiner's construction of Figs. 8A and 8B, 9A and 9B, the multilayered dielectric PCB 40 with an element 42, 142 formed from conductor patterns 46A, 46B and 146A and 146B on a plurality of layers including at least one buried layer of a PCB and the conductor patterns being in a stacked relation and interconnected through the PCB with conductive vias extending through apertures would not be considered by a person of ordinary skill in the art to be a reasonable construction of Holshouser et al. As the Examiner is aware, for anticipation to be proper, the Examiner is required to give the claims their broadest reasonable construction and then must demonstrate that every element of the alleged anticipated claim is found in the reference.

Figs. 8A and 8B of Holshouser et al do disclose a single element 142 which is buried within in the PCB 40, but not at any discernible layer. However, Figs. 9A and 9B do not show this structure. Therefore, it is submitted that the citation of Figs. 9A and 9B by the Examiner as demonstrating anticipation is clearly erroneous since there is no buried layer or antenna element disclosed in those figures.

As may be seen from Fig. 8A as shown by the phantom lines contained therein, the buried structure as shown in Fig. 8B amounts to a series connection of conductive patterns which are connected by vias. It is submitted that a person of ordinary skill in the art would not consider this structure as depicted in Fig. 8A and Fig. B to be in the claimed "stacked relation" since there is only a small amount of overlap between the buried structure which is necessary for the vias to be connected.

Moreover, the Examiner has not demonstrated what constitutes the plurality of layers within the PCB 40. it is submitted that there is only a single dielectric layer having exposed faces on which a conductive pattern 42 is located and further, there is a single buried series connection of conductive elements which at least somewhat overlap the conductive sections of conductor 42. However, such overlap does not include a "conductor patterns on a plurality of layers including at least one buried layer on a multilayer PCB".

A multilayer PCB is understood by persons of ordinary skill in the art to include buried conductor layers as illustrated in Fig. 3. If the Examiner persists in the stated grounds of rejection, it is requested that he define on the record where the "the at least one buried layer of a multilayer PCB" is found since it is submitted that a person of ordinary skill in the art would only consider Holshouser et al as depicted in Figs. 8A and 8B to disclose a PCB which is a multilayered structure.

Furthermore, dependent claims 3 and 4 and 19-20 further recite "the PCB is apertured adjacent to the element". It is submitted that a person of ordinary skill in the art would not consider the conductive vias which fit into holes into the PCB to be

a construction on which the claimed conductive vias and apertures may be read as a single structure as disclosed in Figs. 8A and 8B.

Claims 9-12 and 25-28 stand rejected under 35 U.S.C. §103 as being unpatentable over Holshouser et al in view of United States Patent 5,668,559 (Baro). Baro has been cited as teaching a ground plane conductor performing part of a coaxial feeder and radiator. Baro does not cure the deficiencies noted above with respect to independent claims 1 and 17.

Moreover, claims 11, 12, and 27 and 28 further recite that the "PCB is apertured adjacent to the element" which is patentable for the reasons set forth above with respect to the alleged anticipation of claims 1-4 and 17-20.

In view of the foregoing remarks, it is submitted that each of the claims in the application is in condition for allowance. Accordingly, early allowance thereof is respectfully requested.

To the extent necessary, Applicants petition for an extension of time under 37 C.F.R. §1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 01-2135 (1076.41311X00) and please credit any excess fees to such Deposit Account.

Respectfully submitted,

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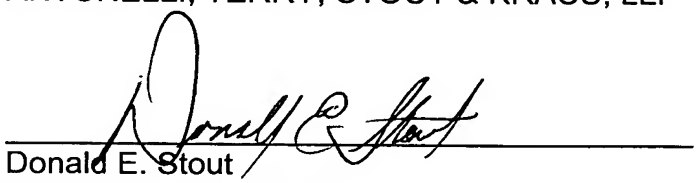

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Attachments

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